IN THE SPECIFICATION

Please replace paragraph [0177] with the following:

FIGS. 12A-12D are simplified illustrations of the formation of a vertical planar semiconductor device in accordance with an embodiment of the present invention. As shown in FIG. 12A, a vertical semiconductor device 900 is provided which includes devices 902, such as transistors, diodes, and the like, formed in the active layer on a first side 904 of semiconductor substrate 906. In one embodiment, the active layer on the first side comprises a material having a low melting point, e.g. in the range of between 100° C and 1400° C.

Please replace paragraph [0185] with the following:

Beneficially, the flash anneal process described above substantially heats only the active layer of second side 908b to the annealing temperature, thus protecting devices 902 formed on first side 904. In one embodiment, the active layer is between 10 nm and 1 mm below the surface of the second side 908b. As illustrated in the graph shown in FIG. 13B, the bulk temperature of the wafer diminishes as a function of the increase in depth towards the second side or opposing surface. Moreover, the more instantaneous the pulse of energy generated by the flash, the less impact to the opposite surface. Thus, although some heat may permeate from the back side through the remainder of the bulk semiconductor substrate, the amount of heat energy which reaches first side 904 can be maintained at a temperature low enough to avoid causing the loss of structural or operational integrity of devices 902.

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